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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Alexander Goldovsky
Case:	9
Serial No.:	To Be Assigned
Filing Date:	December 8, 2000
Title:	Adder With Improved Overflow Flag Generation
Group:	To Be Assigned
Examiner:	To Be Assigned

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying Form PTO-1449. A copy of each listed document is enclosed.

U.S. Patents

U.S. Patent No. 5,581,497 issued on 12/03/96 to Kumar

U.S. Patent No. 5,337,269 issued on 08/09/94 to McMahan et al.

Other Documents

1. A. Weinberger and J.L. Smith, "A One-Microsecond Adder Using One-Megacycle Circuitry," IRE Trans. on Electronic Computers, pp. 65-73, June 1956.

2. T.-F. Ngai et al., "Regular, Area-Time Efficient Carry-Lookahead Adders," Journal of Parallel and Distributed Computing, Vol. 3, pp. 92-105, 1986.

3. P.M. Kogge and H.S. Stone, "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations," IEEE Trans. on Computers, Vol. C-22, No. 8, pp. 786-793, August 1973.

4. R.P. Brent and H.T. Kung, "A Regular Layout for Parallel Adders," IEEE Trans. on Computers, Vol. C-31, No. 3, pp. 260-264, March 1982.

5. D. Dozza et al., "A 3.5 NS, 64 Bit, Carry-Lookahead Adder," in Proc. Intl. Symp. Circuits and Systems, pp. 297-300, 1996.

6. J. Silberman et al., "A 1.0 GHz Single-Issue 64b PowerPC Integer Processor," IEEE Intl. Solid-State Circuits Conf., pp. 230-231, February 1998.

7. W. Liu et al., "A 250-MHz Wave Pipelined Adder in 2-μm CMOS," IEEE Journal of Solid-State Circuits, Vol. 29, No.9, pp. 1117-1128, September 1994.

8. A. Beaumont-Smith et al., "A GaAs 32-bit Adder," IEEE Symposium Computer Arithmetic, pp. 10-17, July 1997.

9. Z. Wang et al., "Fast Adders Using Enhanced Multiple-Output Domino Logic," IEEE Journal of Solid-State Circuits, Vol. 32, No.2, pp. 206-214, February 1997.

10. G. Bewick et al., "Approaching a Nanosecond: A 32 Bit Adder," IEEE International Conference on Computer Design: VLSI in Computers & Processors, pp. 221-226, October 1988.

11. A. Weinberger, "High-Speed Binary Adder," IBM Technical Disclosure Bulletin, Vol. 24, No.8, pp. 4393-4398, January 1982.

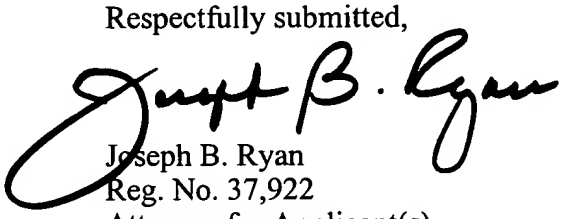
12. S. Knowles, "A Family of Adders," IEEE Symposium Computer Arithmetic, pp. 30-34, 1999.

13. A. Goldovsky et al., "A 1.0-nsec 32-bit Prefix Tree Adder in 0.25-μm Static CMOS," 43rd Midwest Symposium on Circuits and Systems, 5 pages, August 1999.

Applicant's attorney also brings to the attention of the Office the following U.S. Patent Applications: Serial No. 09/291,677 filed April 14, 1999 and entitled "Prefix Tree Adder with Efficient Carry Generation;" Serial No. 09/525,644 filed March 15, 2000 and entitled "Prefix Tree Adder with Efficient Sum Generation;" and Serial No. 09/569,022 filed May 11, 2000 and entitled "Incorporation of Split-Adder Logic within a Carry-Skip Adder without Additional Propagation Delay."

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability, or as a representation that no other material information exists.

Respectfully submitted,



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